



TDC Readout Rate Measurements

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TDWG Meeting



Michigan TDC 101

- Each TDC channel records the state of input signal (0 or 1) once per ns.
- For each L1 accept, the last 2 μ s of data is written into one of four on-chip buffers.
- For each L2 accept, the on-board DSP reads out the appropriate on-chip buffer from each TDC chip (96 total) and creates hit words for each pair of $0 \rightarrow 1$ and $1 \rightarrow 0$ transitions within the appropriate time window.



Michigan TDC 101 (cont.)

- Hit words are loaded into an on-board FIFO and read out by crate processor over the VME backplane.
- Hits observed in each channel outside of the appropriate time window (but within the 2 μ s buffer) must be read out on the older Rev. D boards by the DSP to clear the on-chip buffer.
- On newer Rev. F boards, hits outside the time window can be cleared with a single write.

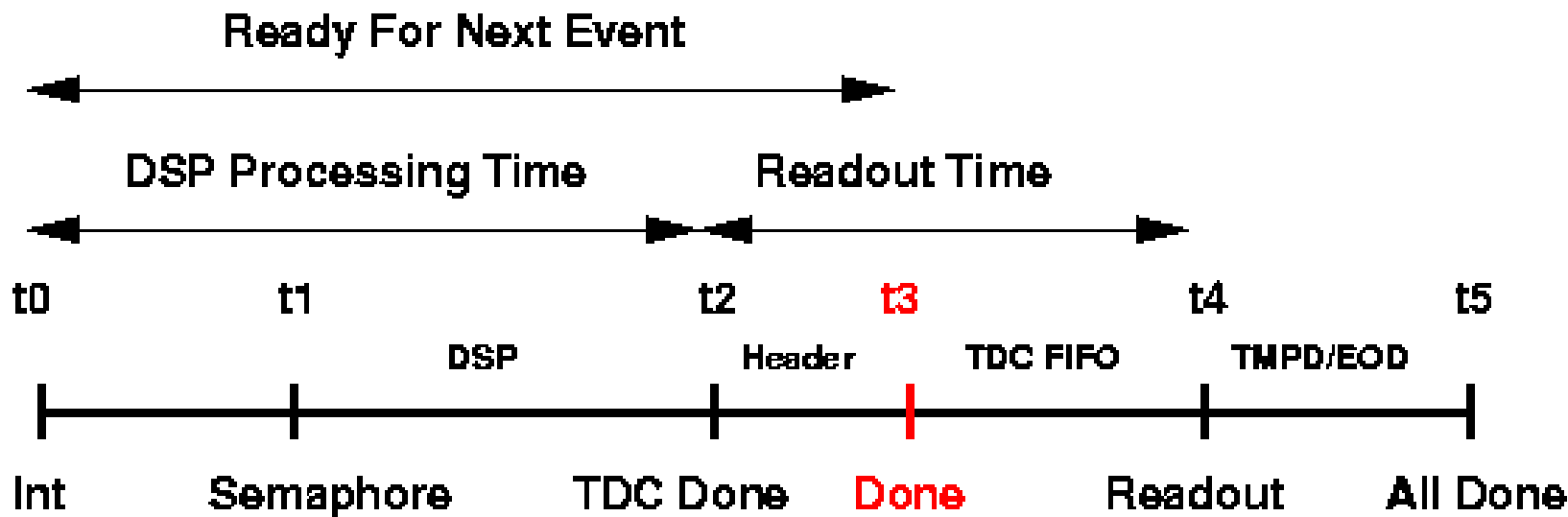


TDC Readout Time

- The total TDC readout time is a combination of DSP processing time and data readout time.
- However, TDC boards are set up to allow the DSP to process one event while the previous event is being readout over the backplane.
- Therefore, the total TDC readout time is roughly equivalent to the larger of the DSP processing or data readout times.



TDC Readout Time (cont.)





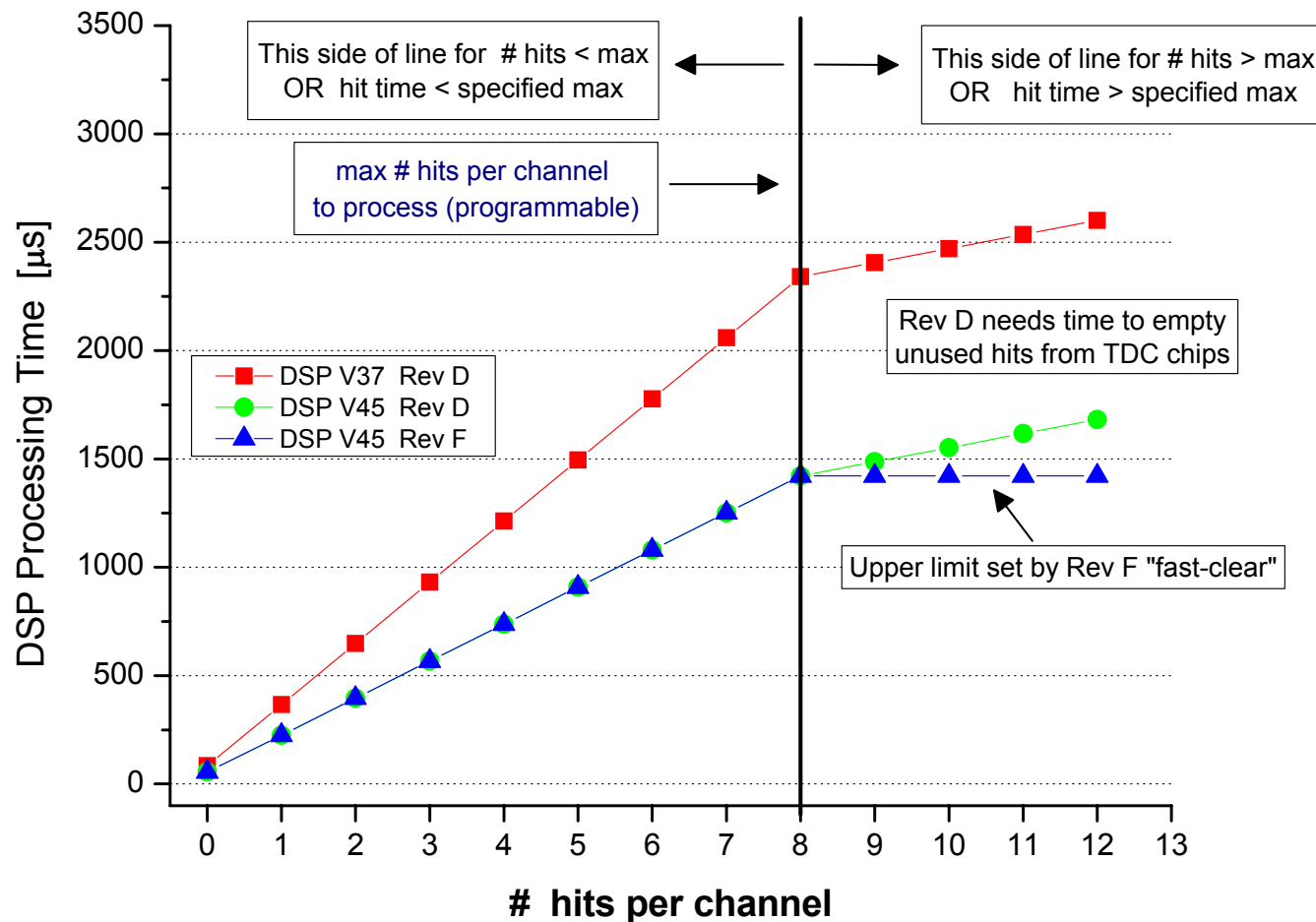
DSP Code Versions

- v37 : Original Version.
- v45 : Direct loading of hit words into FIFO (required changing COTD bank format to place header word after data words). Change front-end code and add padding words to allow for concurrent events in FIFO. Add fast clear.
- v65 : Change COTD data format to allow for roughly a factor of two reduction in number of hit words per events.



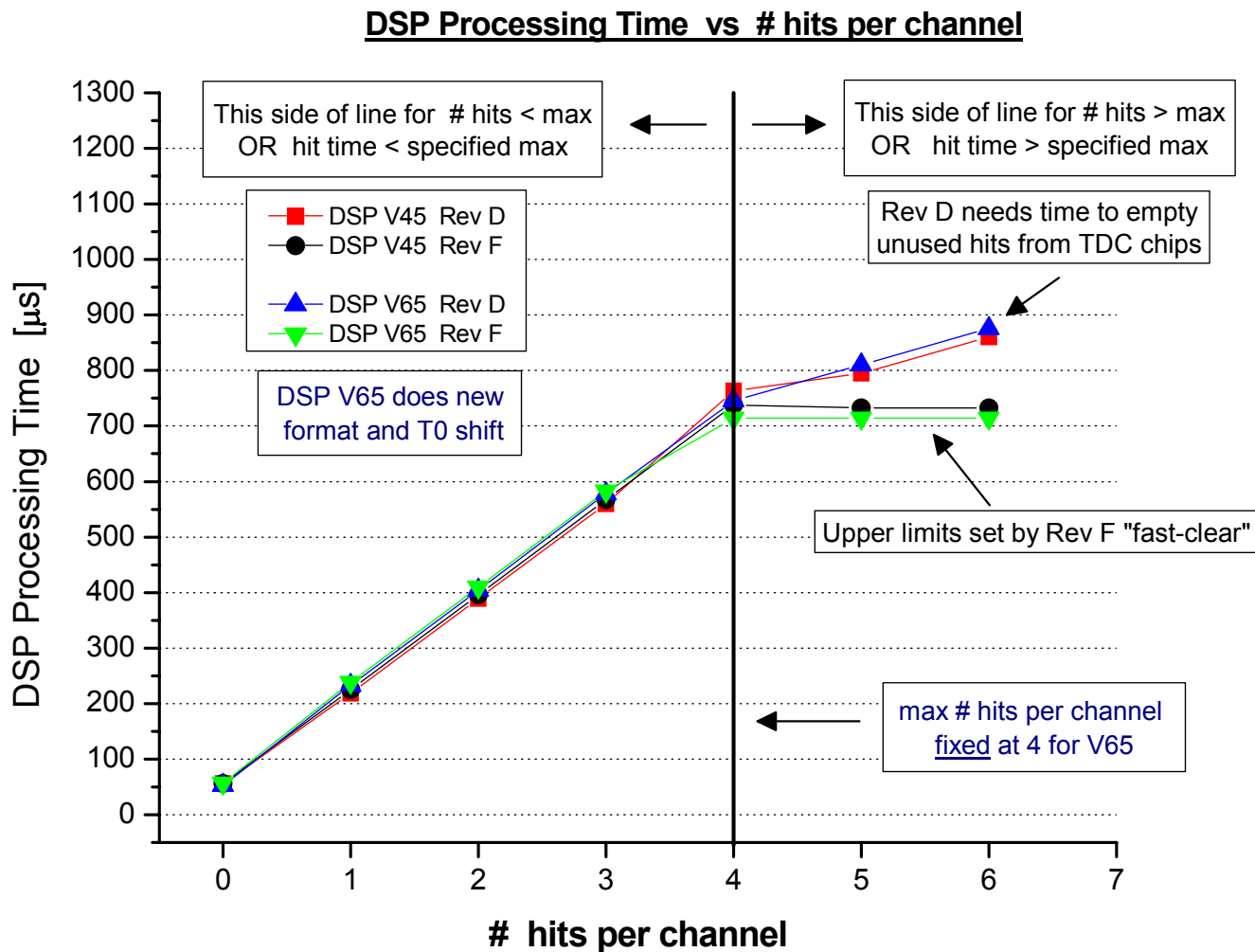
DSP Processing Time (v37 vs. v45)

DSP Processing Time vs # hits per channel



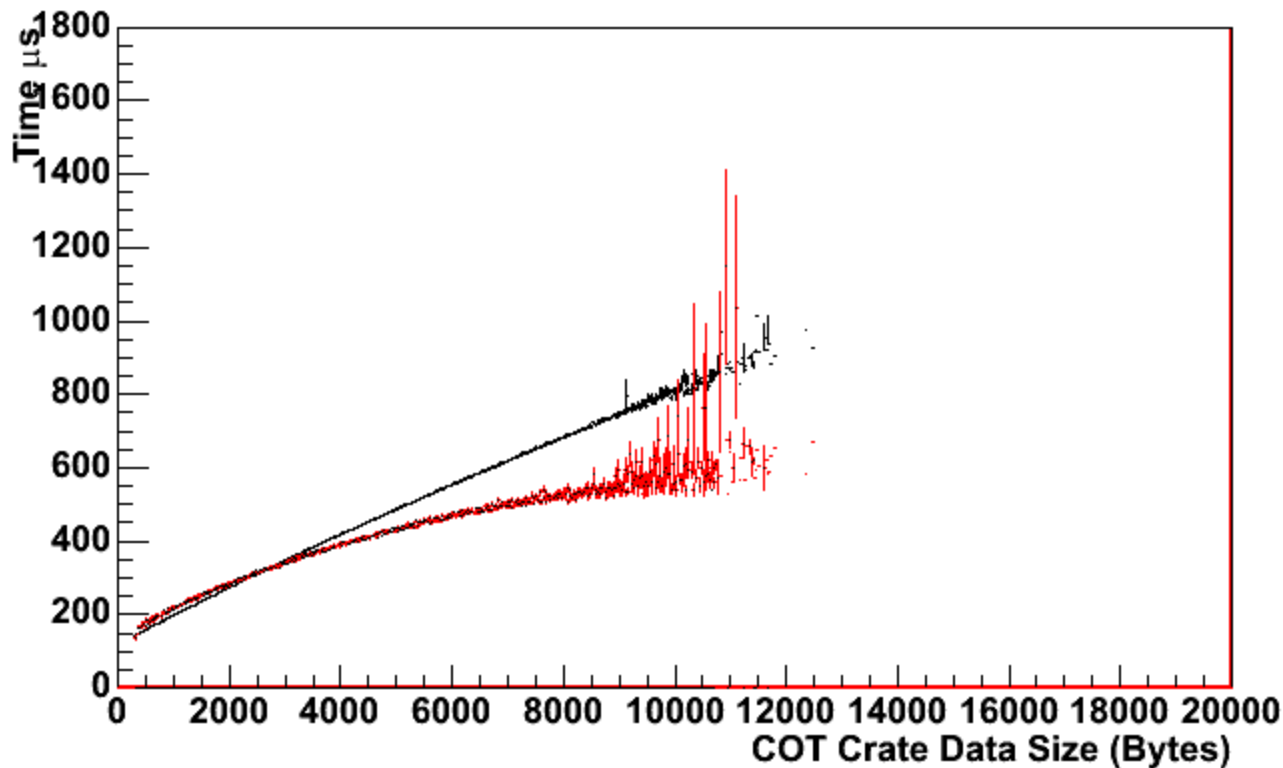


DSP Processing Time (v45 vs. v65)





Timing Measurements from Data



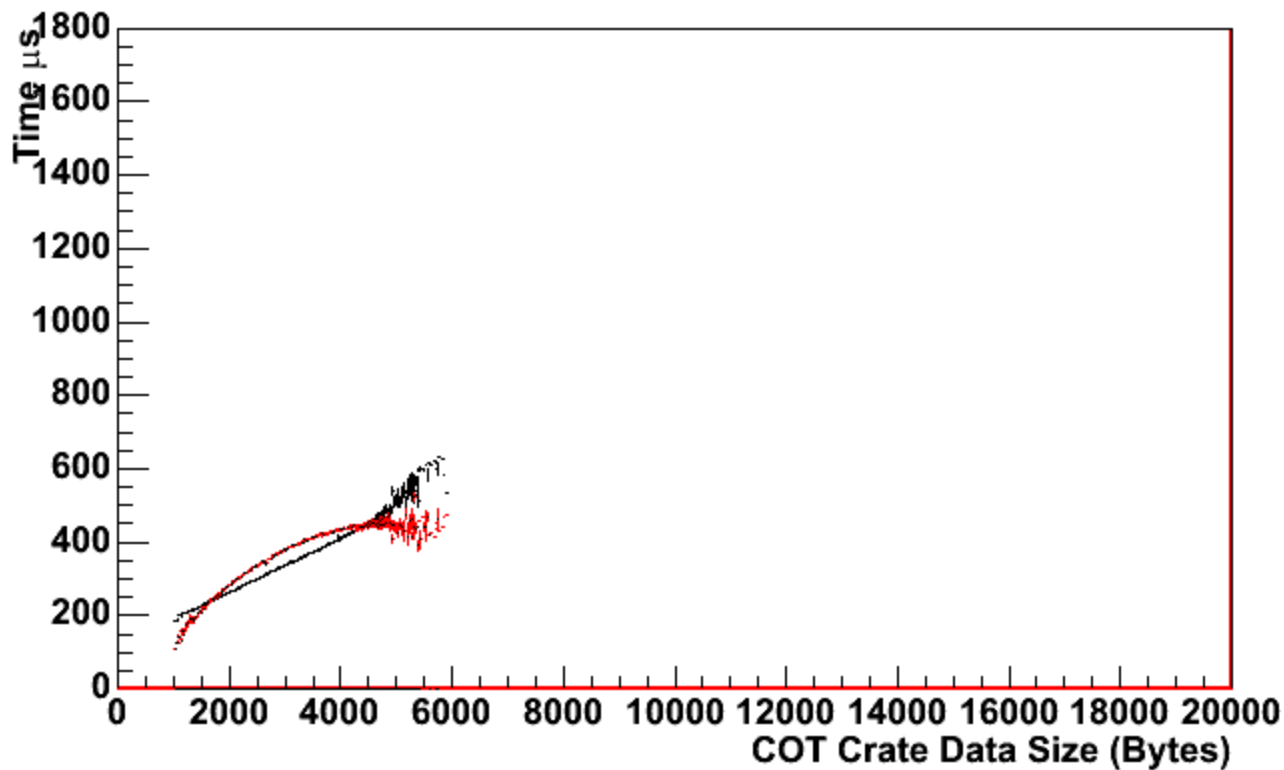
v45

DSP
Processing
Time

Readout
Time



Timing Measurements from Data



v65

DSP
Processing
Time

Readout
Time



Maximum Readout Rate Tests

- Setup a NIM crate to pulse every COT TDC channel with 1-4 pulses within the relevant time window (no hits outside of time window).
- Use two configurations. One where we pulse only the inner four super-layers and a second where we pulse all eight super-layers.
- Use either a constant calibration trigger or a random “sparky” trigger (both rate adjustable).



v45 calibration trigger results

Hits Per Channel	SL 1-4	SL 1-8
1	2424 Hz	1653 Hz
2	1666 Hz	1007 Hz
3	1293 Hz	748 Hz
4	1053 Hz	582 Hz

Maximum
readout rate
with ~100%
deadtime.



v65 calibration trigger results

Hits Per Channel	SL 1-4	SL 1-8
1	2414 Hz	2200 Hz
2	1739 Hz	1596 Hz
3	1374 Hz	1237 Hz
4	1179 Hz	953 Hz

Maximum readout rate with ~100%
deadtime.

Benchmark worst-case
readout rate.



v45 Readout Rate versus Deadtime

L2A (Hz)	L3A (Hz)	Deadtime (%)
400	400	0.75
580	550	4.40
730	640	12.00
950	715	23.00

3 hits/channel
on SL 1-8.

TDC readout contributes minimal deadtime at
L2A \sim 400 Hz even using current DSP v45!



v65 Readout Rate versus Deadtime

L2A (Hz)	L3A (Hz)	Deadtime (%)
496	493	0.49
699	683	2.03
948	880	6.43
1241	1036	15.34
6158	1182	80.65

4 hits/channel
on SL 1-4.



v65 Readout Rate versus Deadtime

L2A (Hz)	L3A (Hz)	Deadtime (%)
503	510	1.05
664	691	3.61
825	941	11.77
914	1233	24.56
956	6146	83.47

4 hits/channel
on SL 1-8.

Unrealistic
worst-case
scenario.



Conclusions

- DSP code v45 is readout time limited. Total TDC readout time has a minimal contribution to overall deadtime at L2A ~ 400 Hz.
- DSP code v65 is DSP processing time limited for realistic data sizes.
- Worst case scenario (4 hits on every channel in at least one TDC on every event) gives maximum readout rates of 1180Hz (100% deadtime) and 880 Hz (5% deadtime).